Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device structure, comprising:

a substrate defining a substantially horizontal plane;

a common source region;

a common drain region;

a gate electrode disposed on said substrate and being electrically insulated therefrom, said gate electrode positioned vertically between said common source region and said common drain region; and

a plurality of semiconducting nanotubes each including a first end physically and electrically coupled with said common source region, a second end physically and electrically coupled with said common drain region, and a channel region extending vertically through said gate electrode between said common source region and said common drain region, said channel region being electrically insulated from said gate electrode, and said gate electrode configured to receive a control voltage effective to regulate current flow through said channel region of a respective one of said semiconducting nanotubes between said common source region and said common drain region.

2. (Currently Amended) The semiconductor device structure of claim 1 wherein said common source is composed of a catalyst material effective for growing said semiconducting nanotubes.

3. (Currently Amended) The semiconductor device structure of claim 1 wherein said common drain is composed of a catalyst material effective for growing said semiconducting nanotubes.

4. (Currently Amended) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said common drain and said gate electrode for electrically isolating said drain from said gate electrode.

5. (Currently Amended) The semiconductor device structure of claim 1 further comprising:

an insulating layer disposed between said common source and said gate electrode for electrically isolating said source from said gate electrode.

6. (Previously Presented) The semiconductor device structure of claim 1 wherein said at least one semiconducting nanotube is composed of arranged carbon atoms.

7. (Cancelled)

8. (Previously Presented) The semiconductor device structure of claim 1 wherein said at least one semiconducting nanotube is oriented substantially perpendicular to said horizontal plane.

9. (Cancelled)

10. (Previously Presented) The semiconductor device structure of claim 1 wherein said gate dielectric is disposed on said semiconducting nanotubes.

11-24. (Cancelled)

25. (Previously Presented) A semiconductor device structure, comprising:

a substrate;

an electrically-conductive first plate on said substrate;

an electrically-conductive second plate disposed vertically above said first plate;

an electrically-conductive layer disposed between said first and second plates;

at least one nanotube having an end electrically coupled with said first plate for increasing an effective area of said first plate, said at least one nanotube positioned in said electrically-conductive layer; and

a dielectric layer coating said length of said at least one nanotube such that said at least one nanotube is electrically isolated from said electrically-conductive layer and said second plate.

26. (Original) The semiconductor device structure of claim 25 wherein said at least one nanotube has a conducting molecular structure.

27. (Original) The semiconductor device structure of claim 25 wherein said at least one nanotube has a semiconducting molecular structure.

28. (Previously Presented) The semiconductor device structure of claim 25 wherein said dielectric layer encases said at least one nanotube.

29-33. (Cancelled)